

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (original) A computer system, comprising:
a processor having a processor bus;
an input device coupled to the processor through the processor bus;
an output device coupled to the processor through the processor bus;
a memory device coupled to the processor bus, the memory device comprising:
a plurality of memory cells;
circuits, clocked by a local clock signal, for writing information into and
reading information out of said memory cells; and
a dual locked loop for locking said local clock signal to an external reference
signal, comprising:
a first locked loop for establishing a phase relationship between said local
clock signal and said reference signal; and
a second locked loop responsive to said first locked loop and comprising:
a delay line having a first portion providing a variable amount of delay
substantially independently of process, temperature and voltage variations and a second
portion in series with said first portion and providing a variable amount of delay that
substantially tracks changes in process, temperature, and voltage variations;
a control circuit for controlling the delay of said delay line;
a phase detector for producing signals for input to said control circuit; and
a feedback path for connecting an output of said delay line to an input of said
first locked loop and to said phase detector, said local clock signal being available at said
output of said delay line.

2. (original) A computer system, comprising:
a processor having a processor bus;

an input device coupled to the processor through the processor bus;
an output device coupled to the processor through the processor bus;
a memory device coupled to the processor bus, the memory device comprising:
a plurality of memory cells;
circuits, clocked by a local clock signal, for writing information into and
reading information out of said memory cells; and
a dual locked loop for locking said local clock signal to an external reference
signal, comprising:
a first locked loop for establishing a phase relationship between said local
clock signal and said reference signal; and
a second locked loop responsive to said first locked loop and comprising:
a first circuit path having a stepwise variable capacitive load;
a second circuit path in series with the first circuit path and having a plurality
of stages each having at least two paths;
a control circuit for controlling the amount of capacitance in said first circuit
path and the number of stages in said second circuit path;
a phase detector for producing signals for input to said control circuit; and
a feedback path for connecting an output of said delay line to an input of said
first locked loop and to said phase detector, said local clock signal being available at said
output of said second locked loop.

3. (cancelled)

4. (currently amended) A computer system, comprising:
a processor having a processor bus;
an input device coupled to the processor through the processor bus;
an output device coupled to the processor through the processor bus;
a memory device coupled to the processor bus, the memory device comprising:
a plurality of memory cells;

circuits, clocked by a local clock signal, for writing information into and reading information out of said memory cells; and

a dual locked loop for locking said local clock signal to an external reference signal, comprising:

a first locked loop for establishing a phase relationship between said local clock signal and said reference signal; and

a second locked loop responsive to said first locked loop and comprising:
a first circuit path having a stepwise variable capacitive load and a second circuit path in series with said first circuit path and having a plurality of stages each having a variable amount of drive associated therewith;

a control circuit for controlling the amount of capacitance in said first circuit path and the number of stages in said second circuit path;

a phase detector for producing signals for input to said control circuit; and

a feedback path for connecting an output of said second locked loop to an input of said first locked loop and to said phase detector, said output signal being available at said output of said second locked loop.

5. (currently amended) A computer system, comprising:

a processor having a processor bus;

an input device coupled to the processor through the processor bus;

an output device coupled to the processor through the processor bus;

a memory device coupled to the processor bus, the memory device comprising:

a plurality of memory cells;

circuits, clocked by a local clock signal, for writing information into and reading information out of said memory cells; and

a dual locked loop for locking said local clock signal to an external reference signal, comprising:

a first locked loop for establishing a phase relationship between said local clock signal and said reference signal; and

a second locked loop responsive to said first locked loop and comprising:

a first circuit path having a plurality of stages each having a variable amount of drive associated therewith and a second circuit path in series with said first circuit path and having a plurality of stages each having at least a fast and a slow path;

a control circuit for controlling the number of stages in said first circuit path and the number of fast paths and slow paths stages in said second circuit path;

a phase detector for producing signals for input to said control circuit; and

a feedback path for connecting an output of said second circuit to an input of said first circuit and to said phase detector.

6. (new) A computer system, comprising:

a processor having a processor bus;

an input device coupled to the processor through the processor bus;

an output device coupled to the processor through the processor bus;

a memory device coupled to the processor bus, the memory device comprising:

a plurality of memory cells;

circuits, clocked by a local clock signal, for writing information into and reading information out of said memory cells; and

a dual locked loop for locking said local clock signal to an external reference signal, comprising:

a first locked loop for establishing a phase relationship between said local clock signal and said reference signal; and

a second locked loop responsive to said first locked loop and comprising:

a delay line having a first portion providing a variable amount of delay with little intrinsic delay and a second portion in series with said first portion and providing a variable amount of delay with a larger intrinsic delay;

a control circuit for controlling the delay of said delay line;

a phase detector for producing signals for input to said control circuit; and

Appl. No.: 10/731,775
Docket No.: DB000861-004
Amdt. Dated: August 19, 2004
Reply to Office action of August 13, 2004

a feedback path for connecting an output of said delay line to an input of said first locked loop and to said phase detector, said local clock signal being available at said output of said delay line.